Q.P. Code: 16EC402 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations December-2021

SWITCHING THEORY & LOGIC DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Convert the following to Decimal and then to Octal. (i) 423416 (ii) 100100112.	**L1**	**6M**
	b	Convert the following to Decimal and then to Hexadecimal. (i) 12348 (ii) 110011112	**L1**	**6M**

OR

2	a	Simplify the following Boolean expressions to minimum no. of literals. i. ABC+A'B+ABC' ii. (BC'+A'D)(AB'+CD') iii. x'yz+xz iv. xy+x(wz+wz')	**L3**	**6M**
	b	Obtain the Dual of the following Boolean expressions. i) AB+A(B+C)+B'(B+D) ii) A+B+A'B'C iii) A'B+A'BC'+A'BCD+A'BC'D'E iv) ABEF+ABE'F'+A'B'EF	**L3**	**6M**

UNIT-II

3		Minimize the given Boolean function F(A,B,C,D) = Σ m(0,1,2,3,6,7,13,15) using tabulation method and implement using basic gates	**L2**	**12M**

OR

4		Simplify the Boolean function by using tabulation method F(a,b,c,d)=Σm(0,1,2,5,6,7,8,9,10,14)	**L3**	**12M**

UNIT-III

5	a	Design & implement a 4-bit Binary-To-Gray code converter	**L3**	**6M**
	b	Design a 4 bit binary-to-BCD code converter	**L3**	**6M**

OR

6	a	Implement the following Boolean function using 8:1 multiplexer. F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D.	**L3**	**6M**
	b	What is multiplexer? Construct 4*1 multiplexer with logic gates and truth table.	**L3**	**6M**

UNIT-IV

7	a	Draw the circuit of JK flip flop using NAND gates and explain its operation	**L3**	**6M**
	b	Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops.	**L1**	**6M**

OR

8		A sequential circuit with two D-flip flops A and B, two inputs 'x' and 'y' and one output 'z' is specified by the following next state and output equation. i) Draw the logic diagram of the circuit. ii) List the state table and draw the corresponding state diagram	**L3**	**12M**

UNIT-V

9		Implement PLA circuit for the following functions F1(A,B,C)=Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7).	L3	12M

OR

10	a	Differentiate among ROM, PROM ,DROM ,EPROM, EEPROM, RAM.	L3	6M
	b	Explain about memory decoding.	L3	6M

*** END ***